A. CLEAN VERSION OF CLAIMS

IN THE CLAIMS:

Please amend claims 1, 22, and 24 as follows:

1. **(Once Amended)** A single transistor ferroelectric memory cell, comprising:

a semiconductor substrate having defined thereon:

a first conductive region of a first conductive type;

a source region of a second conductive type defined in said first conductive region, said source region sized and configured to comprise a portion of the ferroelectric memory cell and an adjacent ferroelectric memory cell; and

a drain region also of a second conductive type defined in said first conductive region, said drain region being spaced apart from said source region such that a channel region comprising a portion of said first conductive region is defined between said source region and said drain region;

a gate oxide layer disposed on said semiconductor substrate to cover the entirety of said drain, channel, and source regions;

a ferroelectric gate unit disposed on said gate oxide layer comprising:

a bottom electrode in electrical communication with said drain region;

a top electrode;

a ferroelectric layer disposed between said bottom and said top electrode; and

a sealing layer disposed on each side of said ferroelectric gate unit; and

an upper conductive layer disposed on said ferroelectric gate unit and a portion of said gate oxide layer such that said upper conductive layer and said top electrode of said ferroelectric gate unit are in electrical communication.

22. **(Once Amended)** A ferroelectric memory cell comprising:

a ferroelectric gate unit comprising a top electrode, a layer of ferroelectric material, and a bottom electrode;

a semiconductor substrate having:

a drain;

a source; and

a channel;

a gate oxide substantially covering the drain, source, and channel; and

means for controlling the polarization of said layer of ferroelectric material.

24. **(Once Amended)** A ferroelectric memory cell as defined in claim 23, wherein the means for controlling the polarization of said layer of ferroelectric material further comprises an upper polysilicon layer deposited on top of said ferroelectric gate unit such that electrical communication is established between said top electrode and said upper polysilicon layer.

B. VERSION OF CLAIMS WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 1, 22, and 24 have been amended as follows:

1. **(Once Amended)** A single transistor ferroelectric memory cell, comprising:

a semiconductor substrate having defined thereon:

a first conductive region of a first conductive type;

a source region of a second conductive type defined in said first conductive region, said source region sized and configured to comprise a portion of the ferroelectric memory cell and an adjacent ferroelectric memory cell; and

a drain region also of a second conductive type defined in said first conductive region, said drain region being spaced apart from said source region such that a channel region comprising a portion of said first conductive region is defined between said source region and said drain region;

a gate oxide layer disposed on said semiconductor substrate to cover **the entirety of** said drain, channel, and source regions;

a ferroelectric gate unit disposed on said gate oxide layer comprising:

a bottom electrode in electrical communication with said drain region;

a top electrode;

a ferroelectric layer disposed between said bottom and said top electrode; and

a sealing layer disposed on each side of said ferroelectric gate unit; and

an upper conductive layer disposed on said ferroelectric gate unit and a portion of said gate oxide [coating] **layer** such that said upper conductive layer and said top electrode of said ferroelectric gate unit are in electrical communication.

22. **(Once Amended)** A ferroelectric memory cell comprising:

a ferroelectric gate unit comprising a top electrode, a layer of ferroelectric material, and a bottom electrode;

a semiconductor substrate having:

a drain;

a source; **and**

a channel;

a gate oxide **substantially covering the drain, source, and channel**; and

means for controlling the polarization of said layer of ferroelectric material.

24. **(Once Amended)** A ferroelectric memory cell as defined in claim 23, wherein the means for controlling the polarization of said layer of ferroelectric material further comprises an upper polysilicon layer deposited on top of said ferroelectric gate unit such that electrical communication is established between said top electrode and said [conducting] **upper** polysilicon layer.